15

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-302963
(43)Date of publication of application : 28.10.1994

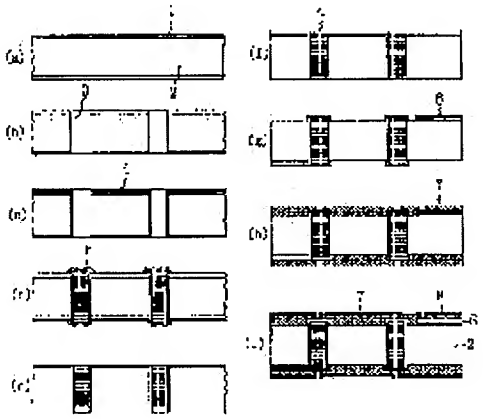
(51)Int.Cl. H05K 3/46
H05K 1/11
H05K 3/40

(21)Application number : 05-086499
(22)Date of filing : 13.04.1993

(71)Applicant : TOKUYAMA SODA CO LTD
(72)Inventor : SHIMAMOTO TOSHIJI

(54) MULTILAYER CIRCUIT BOARD AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To form a high-density wiring pattern with highly reliable through holes by forming a first wiring pattern on the smoothed surface of a conductive layer containing the through holes.
CONSTITUTION: The circuit board uses a copper-clad glass epoxy laminated board as an insulating substrate 2 having conductive layers 1 on both surfaces and, after forming through holes 3 with a drill, plated-copper layers 4 are formed on the internal surfaces of the holes 3 and entire surface of the substrate 2 by electroplating after performing electroless plating. The layers 4 are formed by the electroless plating and electroplating after the holes 3 with the layers 4 are filled with a thermosetting solder resist as a curable insulating resin 5 and the resin 5 is hardened and the surface of the conductive layers 4 containing the curable insulating resin is polished by successively using a No.320 and No.600 buffs. In this multilayer circuit board, therefore, a second wiring pattern 8 can be formed on a first wiring pattern 6 with an insulating layer 7 in between at a high wiring density and with high reliability.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]A conductive layer is formed in a wall of this breakthrough of an insulating substrate that has a breakthrough, and inside of a breakthrough is filled up with insulating hardening resin in which the surface has a smooth side, It consists of a through hole part by which the 1st circuit pattern electrically connected with a conductive layer formed in an inner wall of through hole was formed in this smooth side, and a plate-like part by which the 2nd circuit pattern was formed via an insulating layer on an insulating substrate, A multilayered circuit board to which it as electrically as the 1st circuit pattern of a through hole part comes to connect the 2nd circuit pattern of this plate-like part.
[Claim 2]To this through hole of an insulating substrate which it has to both sides, a conductive layer electrically connected to a wall of a breakthrough by through hole which provided a conductive layer and was formed. After filling up with and hardening hardenability insulating resin, grind smoothly a field constituted by a conductive layer on this surface of an insulating substrate, and cured body of hardenability insulating resin, and form the 1st circuit pattern in the surface subsequently this smoothed, and it ranks second to it, A manufacturing method of a multilayered circuit board forming the 2nd circuit pattern electrically connected with a predetermined portion of the 1st circuit pattern of the above on this insulating layer after forming an insulating layer on an insulating substrate except for a predetermined portion of this 1st circuit pattern.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to a new multilayered circuit board which uses the circuit board to which the circuit pattern formed in both sides of an insulating substrate was electrically connected by the through hole, and a manufacturing method for the same. A multilayered circuit board with the reliability of this through hole able to form a high-density circuit pattern highly in detail and a manufacturing method for the same are provided.
[0002]
[Description of the Prior Art]Conventionally, manufacture of the multilayered circuit board is performed by the method called the mass lamination method or pin lamination method which generally laminates the insulating substrate which has a conductive layer, and copper foil via prepreg to both sides.
[0003]However, since the accumulating press process was used for the described method, heating and a pressurizing press machine were needed, and equipment also had a defect which becomes large-scale. Since it was a batch process, the tendency as for which productivity worsens and substrate cost becomes surely high for the reason continuous running is impossible etc. was suited.
[0004]Then, recent years come and the method of not performing the above accumulating press processes is proposed. For example, it is the method of forming an insulating layer in the double-sided circuit board surface which took the flow, forming the 2nd circuit pattern on this insulating layer by the hardenability conductive resin represented at silver paste, or a plating layer, and manufacturing a multilayered circuit board by a plating through hole.
[0005]
[Problem(s) to be Solved by the Invention]However, although there is a merit referred to as not needing an accumulating press process in the manufacturing method of the multilayered circuit board which forms an insulating layer in the double-sided circuit board surface which took the flow, and forms the 2nd circuit pattern on this insulating layer by the above and a plating through hole, As shown in drawing 2, a through hole must be avoided and formation of an insulating layer and formation of the 2nd circuit pattern must be performed, When the wiring density of the 2nd circuit pattern became very small and considered improvement in the wiring density which is the purpose of the original multilayering, such a method could not necessarily be said to be a rational thing, but there was room of improvement.
[0006]
[Means for Solving the Problem]This invention persons a conductive layer electrically connected to a wall of a breakthrough by through hole which provided a conductive layer and was formed as a result of repeating research wholeheartedly that the above-mentioned problem should be solved to this through hole of an insulating substrate which it has to both sides. By grinding smoothly a conductive layer formed in this insulating-substrate surface, and a field constituted by cured body of hardenability insulating resin, and forming the 1st circuit pattern in the surface subsequently this smoothed, after filling up with and hardening hardenability insulating resin, this -- it finds out that the 2nd circuit pattern can be formed with reliability are high wiring density and sufficient via an insulating layer on the 1st circuit pattern, and came to complete this invention.
[0007]Namely, a conductive layer is formed in a wall of this breakthrough of an insulating substrate in which this invention has a breakthrough, and inside of a breakthrough is filled up with insulating hardening resin in which the surface has a smooth side, It consists of a through hole part by which the 1st circuit pattern electrically connected with a conductive layer formed in an inner wall of through hole was formed in this smooth side, and a plate-like part by which the 2nd circuit pattern was formed via an insulating layer

on an insulating substrate, The 2nd circuit pattern of this plate-like part provides a multilayered circuit board which it as electrically as the 1st circuit pattern of a through hole part comes to connect. To this through hole of an insulating substrate for which this invention has the conductive layer electrically connected to a wall of a breakthrough by through hole which provided a conductive layer and was formed to both sides. After filling up with and hardening hardening insulating resin, grind smoothly a conductive layer formed in this insulating substrate surface, and a field constituted by cured body of hardenability insulating resin, and form the 1st circuit pattern in the surface subsequently this smoothed, and it ranks second to it, After forming an insulating layer on an insulating substrate except for a predetermined portion of this 1st circuit pattern, a manufacturing method of a multilayered circuit board forming the 2nd circuit pattern electrically connected with a predetermined portion of the 1st circuit pattern of the above on this insulating layer is also provided.

[0008]A sectional view of a typical multilayered circuit board of this invention is as being shown in drawing 1 (i). A conductive layer is formed in a wall of this breakthrough of the insulating substrate 2 in which a through hole part of a typical multilayered circuit board of this invention has the breakthrough 3, In a breakthrough, it fills up with insulating hardening resin in which the surface has a smooth side, and the 1st circuit pattern 6 electrically connected with a conductive layer formed in this smooth side at an inner wall of through hole is formed. As for a plate-like part of this multilayered circuit board, the 2nd circuit pattern 8 is formed via the insulating layer 7 on the insulating substrate 2. And this through hole part and a plate-like part are as electrically [the 2nd circuit pattern of this plate-like part] as the 1st circuit pattern of a through hole part connected. This multilayered circuit board is carrying out shape which generally has two or more through hole parts. The 1st circuit pattern that the 2nd circuit pattern does not electrically need to be connected with the 1st circuit pattern in all these through hole parts, and was provided in an upper bed and a lower end of this through hole part does not necessarily need to be altogether connected with the 2nd circuit pattern. It is not necessarily indispensable to form the 1st circuit pattern in both sides, and what is necessary is just to choose formation of the 1st circuit pattern if needed, although it is common to form the 1st circuit pattern in both sides of an upper bed of this through hole part and a lower end similarly.

[0009]An insulating substrate in particular used in this invention is not restricted, but is used without restriction of what has publicly known construction material and structure. If a typical thing is illustrated, a paper base-phenol resin laminated circuit board, a paper base-epoxy resin laminated circuit board, A paper base-polyester resin laminated circuit board, a glass base material-epoxy resin laminated circuit board, A paper base-Teflon-resin laminated circuit board, a glass base material-polyimide resin laminated circuit board, A glass base material-BT (bismaleimide triazine) resin resin laminated circuit board, A metal system insulating substrate which covered and carried out the insulation process of the metal, such as flexible substrates, such as synthetic resin bases, such as a composite resin substrate, polyimide resin, polyester resin, aluminum, iron, stainless steel, with an epoxy resin etc., or a ceramics board is mentioned.

[0010]The above-mentioned insulating substrate has a conductive layer for pattern formation to both sides. Construction material in particular of this conductive layer for pattern formation is not restricted. If typical construction material is illustrated, copper, nickel, aluminum, etc. will be mentioned. Although not restricted in particular about thickness of the above-mentioned conductive layer for pattern formation, either, generally 5-70 micrometers is suitable.

[0011]In order that a multilayered circuit board of this invention may electrically connect the above-mentioned conductive layer for pattern formation, a conductive layer for through holes is formed in a wall of an insulating substrate, and a through hole is provided. Construction material of this conductive layer for through holes and a formation method in particular for the same are not restricted. Generally, what has construction material [be / the same as that of a conductive layer for pattern formation / it] is used. If a thing typical as a formation method is illustrated, a method by plating is preferred. especially even if a conductive layer formed in this wall thickness-sees and it attaches, it is not restricted, but generally 5-30 micrometers is suitable.

[0012]A path in particular of the above-mentioned through hole is not restricted, and can be set up arbitrarily. What is necessary is for more than an aperture that is a grade which can generally be filled up with hardenability insulating resin just to usually adjust preferably 0.2 mm or more, so that it may be set to 0.3-2 mm.

[0013]A multilayered circuit board of this invention makes the above-mentioned through hole fill up with and harden hardenability insulating resin, before forming a circuit pattern in a conductive layer for pattern formation. As this hardenability insulating resin, a filler or a thing mixed with an organic solvent is used for hardening resin of cross-linking, such as an epoxy resin, phenol resin, and an acrylic resin, if needed, and it

can be used, choosing from publicly known hardenability insulating resin which has the above-mentioned presentation generally. What gives a cured body in which these hardenability insulating resin is not substantially dissolved by etching reagent is used suitably. By being filled up with a cured body which is not substantially dissolved in this etching reagent in this through hole, in a circuit pattern formation process which is a post process, there is an effect which protects a conductive layer for through holes from an etching reagent, and the reliability of this conductive layer for through holes can be improved. Since inside of a through hole is filled with this insulating resin and liquefied etching resist can be used, formation of an etching resist layer by screen printing is possible, and it is dramatically advantageous to fertilization.

[0014]This hardenability insulating resin fills the whole space of a through hole, and from both the surfaces of a conductive layer, restoration to a through hole of an insulating substrate of the above-mentioned hardenability insulating resin will not be restricted, especially if it is a method with which it is specifically preferably filled up 0.05 mm or more a little to such an extent that it projects 0.1-2 mm. A method of performing spreading of 1 time or multiple times by print processes if a typical method of being filled up with this hardenability insulating resin is illustrated, It is filled up by a method, a roll coater, or a curtain coating machine pressed fit by a squeegee of a rear surface couple from the rear surface both-sides side of an insulating substrate, and means, such as the method of scratching an excessive paint by a squeegee, are used suitably.

[0015]What is necessary is for hardening of hardenability insulating resin with which a through hole was filled up to choose suitably a thing suitable for hardening of hardenability conductive material, and just to stiffen it from publicly known curing methods, such as a hot blast stove, an infrared furnace, a far-infrared furnace, an ultraviolet curing furnace, and electron beam curing oven.

[0016]It is important to grind smoothly the surface constituted by cured body of a conductive layer and hardenability insulating resin after hardening hardenability insulating resin with a described method. Namely, by this grinding, in formation of a circuit pattern which is a post process, formation of a pattern by etching resist and etching can be performed with sufficient accuracy, and an insulating layer to this circuit pattern top can also be formed with sufficient reliability. Generally a method used for polish usual [, such as slurry polish, buffing, and scrub polish,] as a method of grinding smoothly the surface constituted with a conductive layer and hardenability insulating resin is used.

[0017]The 1st circuit pattern is formed on a field where a conductive layer containing the above-mentioned through hole portion was smoothed. A formation method of this circuit pattern has a common method of forming an etching pattern in the smoothed field by etching resist, and subsequently etching.

[0018]When a metal skin is formed on a field where a conductive layer containing the above-mentioned through hole portion was smoothed, by formation of this metal skin. A flow of the above-mentioned circuit pattern and the 2nd circuit pattern through an insulating layer can be taken on a through hole, and it becomes possible to improve wiring density of a multilayered circuit board by leaps and bounds. A formation method of this metal skin can be performed with a chemical-plating method or an electroplating method. Although construction material of this metal skin is used without restricting a publicly known conductive metal in particular, it is preferred to choose the same construction material as conductive metals, such as copper used as construction material of hardenability conductive material which generally gives a cured body which has the above-mentioned conductivity. Although restriction in particular is not carried out, thickness of a metal skin is usually 50 micrometers or less in thickness, and is good to carry out at 5 micrometers - about 35 micrometers preferably.

[0019]Especially, the aforementioned etching resist is used without restriction, and a dry film, resist ink, etc. should just use it by fine degree of a pattern, choosing it suitably. The etching resist pattern should just adopt a positive pattern or a negative pattern suitably with an etching method. For example, what is necessary is just to adopt a negative pattern in an etching method represented with an etching method represented by tenting by the solder exfoliating method and the SES method in a positive pattern.

[0020]An insulating layer is formed on the 1st [of a multilayered circuit board of this invention] circuit pattern. The above-mentioned insulating layer is formed except for predetermined portions of the 2nd circuit pattern that carries out a postscript, and the 1st circuit pattern electrically connected. A grade which can take an electrical link with the 1st circuit pattern, the 2nd circuit pattern, and a through hole may be sufficient as a size of a portion exposed from an insulating layer, and if it illustrates concretely, not less than 50 micrometers of nominal diameters [not less than 100 micrometers of] should just expose it preferably. Shape in particular of a portion to expose is not limited, but should just adopt suitably circular, a rectangle, and shape of having been suitable for a design of a square equidistant placement line pattern.

[0021]A formation method in particular of an insulating layer is not limited, but a publicly known method is adopted without restriction. A method which generally uses hardenability insulating resin of various

gestalten, such as a dry film, liquid resist, a dry film, and liquid resist concomitant use, is adopted. It is the above-mentioned method, and if especially a dry film is used, thickness accuracy of an insulating resin layer is also good, and since it can form in a table and rear-face coincidence, an insulating layer can be formed more efficiently. What is necessary is just to adopt print processes, a photographic method, etc. suitably by fine degree as the imaging method of this insulating layer.

[0022]The 2nd circuit pattern is formed on the above-mentioned insulating layer. In a predetermined portion of the 1st circuit pattern exposed from an insulating layer, a flow with this 2nd circuit pattern and 1st circuit pattern can be performed. A flow with the 2nd circuit pattern on a side front, the 1st circuit pattern on the back side, and the 2nd circuit pattern, What is necessary is just to have carried out via a portion exposed from an insulating layer on a through hole, and like before, this through hole did not need to be avoided, a beer hall for connection did not need to be established in the neighborhood, and it became possible to make wiring density of the 2nd circuit pattern high.

[0023]It is used especially as the 2nd above-mentioned circuit pattern, without being restricted to patterns, such as a signal wire, a power source wire, a ground wire, and an electromagnetic wave shield layer. Although a method in particular of forming a circuit pattern to an insulating-layer top is not restricted, it is a method, electroless deposition, electroplating, etc. which are formed by print processes etc. using hardenability conductive material represented by copper paste, silver paste, etc., A method of forming a metal skin on all the substrates containing an insulating layer, and etching this metal skin and forming a pattern, etc. are common.

[0024]The multilayered circuit board of this invention can still laminate an insulating layer and a circuit pattern one by one similarly on said 2nd circuit pattern.

[0025]In this invention, it is also possible to laminate an obtained multilayered circuit board via prepreg, and also to carry out the Kota stratification.

[0026]

[Effect of the Invention]According to the manufacturing method of the multilayered circuit board of this invention, smoothly, since the conductive layer containing the through hole portion formed in the insulating substrate is ground, The 1st circuit pattern can be formed on this conductive layer, and formation of an insulating layer and the 2nd circuit pattern can be further performed with certainly and sufficient accuracy on this circuit pattern, and can obtain a reliable laminated circuit board, and. Since connection between the 2nd circuit pattern and a through hole can be directly made on this through hole, it has the feature that a multilayer interconnection board is obtained with high wiring density.

[0027]

[Example]Hereafter, in order to explain this invention concretely, an example is shown, but this invention is not limited to these examples.

[0028]The circuit board was manufactured according to the process shown in example 1 drawing 1. That is, as the insulating substrate 2 which has the conductive layer 1, the 1.6-mm-thick glass epoxy copper-clad laminate sheet was used for (a) both sides, and the breakthrough 3 with a (b) diameter [phi] of 0.4 mm was formed in them by drilling. (c) After performing electroless plating to this breakthrough and an entire substrate, electroplating was given to them and the 25-micrometer-thick copper plating layer 4 was formed in them. (d) To the breakthrough in which the plating layer was formed, the commercial thermosetting solder resist was filled up with and hardened with screen printing as the hardenability insulating resin 5. (e) The buff of No. 320 and No. 600 was used one by one, and polish counter etching of the conductive layer surface containing this hardenability insulating resin was carried out. (f) Next, this electroless plating and electroplating were given and the 15-micro-thick plating layer 4 was formed. (g) Etching resist ink was used, the etching resist layer was formed, it etched into the above-mentioned plating layer surface with the ferric chloride etching solution, the etching resist layer was exfoliated on it, and the 1st circuit pattern 6 was formed in it. (h) this -- on the 1st circuit pattern, photosensitive insulation resist was applied and developed [exposed and] as the insulating layer 7, and the insulating layer was formed. Next, electroless deposition and electroplating were performed to the (i) substrate face, and the 10-micrometer-thick metal skin was formed in it. Subsequently, the 2nd circuit pattern 8 was formed according to the process of the above (g).

[0029]JIS and the hot oil examination (20 **x 20 seconds <- ->260 ** cycle of 5 seconds) of C-5012 were carried out about between the 2nd circuit pattern linked to the through hole which locates and is common in the rear surface of the obtained multilayered circuit board. Even in 500 times of the numbers of cycles, the flow between the 2nd circuit pattern located in the rear surface of the above-mentioned multilayered circuit board is taken, and the rise of resistance was not seen.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]Drawing 1 is process drawing showing the typical mode of the method of this invention.
[Drawing 2]Drawing 2 is a sectional view of the multilayered circuit board obtained by conventional technology.
[Description of Notations]
1 Conductive layer
2 Insulating substrate
3 Breakthrough
4 Plating layer
5 Hardenability insulating resin
6 The 1st circuit pattern
7 Insulating layer
8 The 2nd circuit pattern

[Translation done.]

* NOTICES *

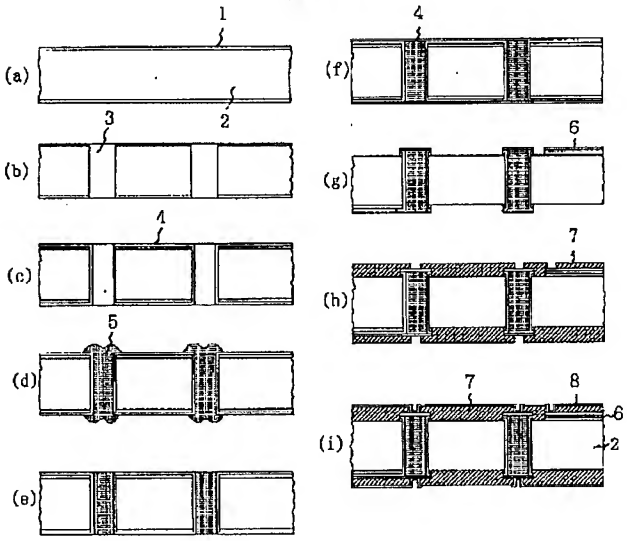
1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

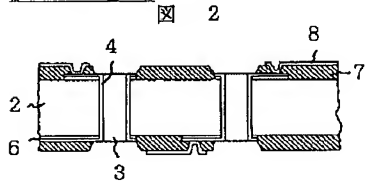
[Drawing 1]

図 1



[Drawing 2]

図 2



[Translation done.]

Filing info	Patent H05-086499 (13.4.1993)
Publication info	H06-302963 (28.10.1994)
Detailed info of application	Kind of final decision(Deemed to be withdrawn) Date of final decision in examination stage(25.7.2000)
Renewal date of legal status	(29.6.2001)

Legal status information includes 8 items below. If any one of them has any data, a number or a date would be indicated at the relevant part.

1. Filing info(Application number,Filing date)
2. Publication info(Publication number,Publication date)
3. Detailed info of application
   * Kind of examiner's decision
   * Kind of final decision
   * Date of final decision in examination stage
4. Date of request for examination
5. Date of sending the examiner's decision of rejection(Date of sending the examiner's
6. Appeal/trial info
   * Appeal/trial number,Date of demand for appeal/trial
   * Result of final decision in appeal/trial stage,Date of final decision in appeal/tria
7. Registration info
   * Patent number,Registration Date
   * Date of extinction of right
8. Renewal date of legal status

For further details on Legal-Status, visit the following link.PAJ help(1-5)

【物件名】　刊行物２

【添付書類】

刊行物（２）

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号
特開平6－302963
(43)公開日　平成６年(1994)10月28日

(51)Int.Cl.⁵		識別記号	庁内整理番号	F I	技術表示箇所
H05K	3/46	N	6921－4E		
		B	6921－4E		
	1/11	H	7511－4E		
	3/40	Z	7511－4E		

審査請求　未請求　請求項の数２　ＯＬ　（全５頁）

(21)出願番号　特願平5－86499

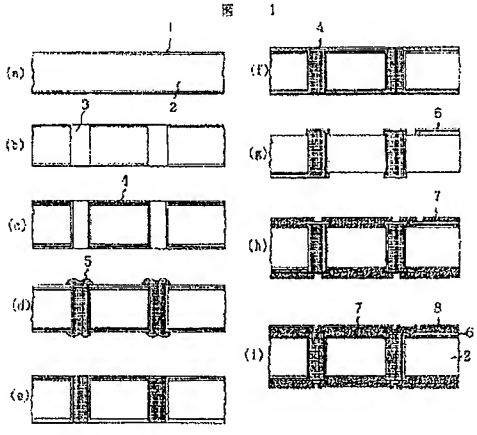
(22)出願日　平成５年(1993)４月13日

(71)出願人　000003182
株式会社トクヤマ
山口県徳山市御影町１番１号
(72)発明者　島本　敏次
山口県徳山市御影町１番１号　徳山曹達株式会社内

(54)【発明の名称】　多層回路基板及びその製造方法

(57)【要約】
【構成】　貫通孔を有する絶縁基板の該貫通孔の内壁に導電層が形成されており且つ貫通孔内はその表面が平滑面を有する絶縁硬化樹脂で充填されており、該平滑面に貫通孔内壁に形成した導電層と電気的に接続する第１の配線パターンが形成されたスルーホール部と絶縁基板上に絶縁層を介して第２の配線パターンが形成された板状部とよりなり、該板状部の第２の配線パターンはスルーホール部の第１の配線パターンと電気的に接続されてなる多層回路基板。
【効果】　本発明の多層回路基板の製造方法によれば、絶縁基板に形成されたスルーホール部分を含む導電層が平滑に、研削されているので、該導電層上に第１の配線パターンを形成し、更に該配線パターンの上に、絶縁層及び第２の配線パターンの形成を確実に且つ精度よく行い、信頼性の高い積層回路基板を得ることができると共に、第２の配線パターンとスルーホールとの接続を該スルーホール上で直接行うことができるため、高い配線密度で多層配線基板が得られるという特徴を有する。

図　1



【特許請求の範囲】

【請求項１】　貫通孔を有する絶縁基板の該貫通孔の内壁に導電層が形成されており且つ貫通孔内はその表面が平滑面を有する絶縁硬化樹脂で充填されており、該平滑面に貫通孔内壁に形成した導電層と電気的に接続する第１の配線パターンが形成されたスルーホール部と絶縁基板上に絶縁層を介して第２の配線パターンが形成された板状部とよりなり、該板状部の第２の配線パターンはスルーホール部の第１の配線パターンと電気的に接続されてなる多層回路基板。

【請求項２】　貫通孔の内壁に導電層を設けて形成されたスルーホールによって電気的に接続された導電層を両面に有する絶縁基板の該スルーホールに、硬化性絶縁樹脂を充填して硬化した後、該絶縁基板表面の導電層と硬化性絶縁樹脂の硬化体によって構成される面を平滑に研削し、次いで該平滑化された表面に第１の配線パターンを形成し、次いで、該第１の配線パターンの所定の部分を除いて絶縁基板上に絶縁層を形成した後、上記第１の配線パターンの所定の部分と電気的に接続する第２の配線パターンを該絶縁層上に形成することを特徴とする多層回路基板の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、絶縁基板の両面に形成された配線パターンがスルーホールにより電気的に接続された回路基板を用いてなる新規な多層回路基板及びその製造方法に関する。詳しくは、該スルーホールの信頼性が高く、且つ、高密度の配線パターンを形成することが可能な多層回路基板及びその製造方法を提供するものである。

【０００２】

【従来の技術】従来、多層回路基板の製造は、一般に、両面に導電層を有する絶縁基板や銅箔をプリプレグを介して積層する、マスラミネーション方式或いはピンラミネーション方式と呼ばれる方法で行われている。

【０００３】しかし上記方法は、積層プレス工程を用いているため、加熱・加圧プレス機が必要となり、設備も大がかりになる欠陥があった。またバッチ工程であるため連続運転が出来ない等の理由により生産性が悪く、基板コストがどうしても高くなる傾向にあった。

【０００４】そこで、近年になって、上記のような積層プレス工程を行わない方法が提案されている。例えば、鍍金スルーホールによって導通をとった両面回路基板表面に絶縁層を形成し、該絶縁層上に第２の配線パターンを銀ペーストに代表される硬化性導電性樹脂、或いは、鍍金層で形成し、多層回路基板を製造する方法である。

【０００５】

【発明が解決しようとする課題】ところが、上記、鍍金スルーホールによって導通をとった両面回路基板表面に絶縁層を形成し、該絶縁層上に第２の配線パターンを形成してなる多層回路基板の製造方法においては、積層プレス工程を必要としないと言ったメリットはあるが、図２に示すように、スルーホールを避けて、絶縁層の形成及び第２の配線パターンの形成を行わねばならず、第２の配線パターンの配線密度が極めて、小さくなってしまい、当初の多層化の目的である配線密度の向上を考えると、このような方法は必ずしも合理的なものとは言えず、改良の余地があった。

【０００６】

【課題を解決するための手段】本発明者らは、上記の問題を解決すべく鋭意研究を重ねた結果、貫通孔の内壁に導電層を設けて形成されたスルーホールによって電気的に接続された導電層を両面に有する絶縁基板の該スルーホールに、硬化性絶縁樹脂を充填して硬化した後、該絶縁基板表面に形成された導電層と硬化性絶縁樹脂の硬化体によって構成される面を平滑に研削し、次いで該平滑化された表面に第１の配線パターンを形成することにより、該第１の配線パターン上に絶縁層を介して、第２の配線パターンを高い配線密度で、且つ、信頼性よく形成できることを見いだし本発明を完成するに至った。

【０００７】即ち、本発明は、貫通孔を有する絶縁基板の該貫通孔の内壁に導電層が形成されており且つ貫通孔内はその表面が平滑面を有する絶縁硬化樹脂で充填されており、該平滑面に貫通孔内壁に形成した導電層と電気的に接続する第１の配線パターンが形成されたスルーホール部と絶縁基板上に絶縁層を介して第２の配線パターンが形成された板状部とよりなり、該板状部の第２の配線パターンはスルーホール部の第１の配線パターンと電気的に接続されてなる多層回路基板を提供する。また、本発明は、貫通孔の内壁に導電層を設けて形成されたスルーホールによって電気的に接続された導電層を両面に有する絶縁基板の該スルーホールに、硬化絶縁性樹脂を充填して硬化した後、該絶縁性基板表面に形成された導電層と硬化性絶縁樹脂の硬化体によって構成される面を平滑に研削し、次いで該平滑化された表面に第１の配線パターンを形成し、次いで、該第１の配線パターンの所定の部分を除いて絶縁基板上に絶縁層を形成した後、上記第１の配線パターンの所定の部分と電気的に接続する第２の配線パターンを該絶縁層上に形成することを特徴とする多層回路基板の製造方法をも提供するものである。

【０００８】本発明の代表的な多層回路基板の断面図は図１（ｉ）に示す通りである。本発明の代表的な多層回路基板のスルーホール部は貫通孔３を有する絶縁基板２の該貫通孔の内壁に導電層が形成されており、貫通孔内はその表面が平滑面を有する絶縁硬化樹脂で充填されており、該平滑面に貫通孔内壁に形成した導電層と電気的に接続する第１の配線パターン６が形成されている。また、該多層回路基板の板状部は絶縁基板２上に絶縁層７を介して第２の配線パターン８が形成されている。そし

て該スルーホール部と板状部とは該板状部の第２の配線パターンがスルーホール部の第１の配線パターンと電気的に接続されている。該多層回路基板は一般に複数のスルーホール部を有する形状をしている。かかる全てのスルーホール部において第２の配線パターンが第１の配線パターンと電気的に接続されている必要はなく、また該スルーホール部の上端と下端に設けられた第１の配線パターンが必ずしも全て第２の配線パターンと接続されている必要もない。同様に該スルーホール部の上端と下端との両面に第１の配線パターンを形成するのが一般的であるが、必ずしも両面に第１の配線パターンを形成することが必須ではなく、必要に応じて第１の配線パターンの形成を選べばよい。

【０００９】本発明において用いる絶縁基板は特に制限されず、公知の材質、構造を有するものが制限無く使用される。代表的なものを例示すれば、紙基材－フェノール樹脂積層基板、紙基材－エポキシ樹脂積層基板、紙基材－ポリエステル樹脂積層基板、ガラス基材－エポキシ樹脂積層基板、紙基材－テフロン樹脂積層基板、ガラス基材－ポリイミド樹脂積層基板、ガラス基材－ＢＴ（ビスマレイミドートリアジン）レジン樹脂積層基板、コンポジット樹脂基板等の合成樹脂基板や、ポリイミド樹脂、ポリエステル樹脂等のフレキシブル基板や、アルミニウム、鉄、ステンレス等の金属をエポキシ樹脂等で覆って絶縁処理した金属系絶縁基板、あるいはセラミックス基板等が挙げられる。

【００１０】上記の絶縁基板は両面にパターン形成用導電層を有する。このパターン形成用導電層の材質は特に制限されない。代表的な材質を例示すれば、銅、ニッケル、アルミニウム等が挙げられる。又、上記パターン形成用導電層の厚みについても特に制限されないが、一般には５～７０μｍが適当である。

【００１１】本発明の多層回路基板は、上記のパターン形成用導電層を電気的に接続するために、絶縁基板の内壁にスルーホール用導電層を形成してスルーホールが設けられる。該スルーホール用導電層の材質及びその形成方法は、特に制限されない。一般に、材質は、パターン形成用導電層と同様のものが使用される。また、形成方法として代表的なものを例示すれば、鍍金による方法が好ましい。また、該内壁に形成される導電層の厚みついても特に制限されないが、一般には、５～３０μｍが適当である。

【００１２】また、上記スルーホールの径は、特に制限されるものではなく、任意に設定することができる。一般に、硬化性絶縁樹脂を充填することが可能な程度の孔径以上、通常０．２ｍｍ以上、好ましくは、０．３～２ｍｍとなるように調節すれば良い。

【００１３】本発明の多層回路基板は、パターン形成用導電層に配線パターンを形成する前に、上記スルーホールに硬化性絶縁樹脂を充填して硬化させる。該硬化性絶縁樹脂としては、エポキシ樹脂、フェノール樹脂、アクリル樹脂等の架橋性の硬化性樹脂に、必要に応じて、フィラー或いは、有機溶剤と共に混合したものが使用され、一般には、上記組成を有する公知の硬化性絶縁樹脂より選択して使用することができる。これらの硬化性絶縁樹脂は、エッチング液により実質的に溶解されない硬化体を与えるものが好適に使用される。かかるエッチング液に実質的に溶解されない硬化体を、該スルーホール内に充填することにより、後工程である、配線パターン形成工程において、スルーホール用導電層をエッチング液より保護する効果があり、該スルーホール用導電層の信頼性を高めることができる。更に、スルーホール内が該絶縁樹脂で満たされているため、液状のエッチングレジストを使用することができるため、スクリーン印刷法によるエッチングレジスト層の形成が可能であり、量産化に対し非常に有利である。

【００１４】上記硬化性絶縁樹脂の絶縁基板のスルーホールへの充填は、該硬化性絶縁樹脂がスルーホールの全空間を満たし、且つ導電層の両表面より若干、具体的には、０．０５ｍｍ以上、好ましくは、０．１～２ｍｍ突出する程度に充填する方法であれば特に制限されない。該硬化性絶縁樹脂の代表的な充填法を例示すれば、印刷法によって１回或いは複数回の塗布を行う方法、絶縁基板の表裏両面側から表裏一対のスキージで圧入する方法、ロールコーター或いはカーテンコーターによって充填し、余分の塗料をスキージで掻き取る方法等の手段が好適に用いられる。

【００１５】また、スルーホールに充填された硬化性絶縁樹脂の硬化は、熱風炉、赤外線炉、遠赤外線炉、紫外線硬化炉、電子線硬化炉等の公知の硬化方法より、硬化性導電物質の硬化に適するものを適宜選んで硬化させれば良い。

【００１６】上記方法によって硬化性絶縁樹脂を硬化後、導電層及び硬化性絶縁樹脂の硬化体によって構成される表面を平滑に研削することが重要である。即ち、かかる研削により、後工程である配線パターンの形成において、エッチングレジストによるパターンの形成、及びエッチングを精度良く行うことができ、且つ該配線パターン上への絶縁層をも信頼性よく形成することができる。導電層及び硬化性絶縁樹脂によって構成される表面を平滑に研削する方法としては、スラリー研磨、バフ研磨、スクラブ研磨等の通常の研磨に用いられる方法が一般に用いられる。

【００１７】上記スルーホール部分を含む導電層の平滑化された面上には、第１の配線パターンが形成される。該配線パターンの形成方法は、その平滑化された面にエッチングレジストによりエッチングパターンを形成し、次いでエッチングを行う方法が一般的である。

【００１８】上記スルーホール部分を含む導電層の平滑化された面上に、メッキ層が形成される場合、かかるメ

ッキ層の形成で、上記配線パターンと絶縁層を介した第２の配線パターンの導通をスルーホール上でとることができ、多層回路基板の配線密度を飛躍的に向上することが可能となる。該メッキ層の形成方法は、化学メッキ法或いは、電気メッキ法で行うことができる。該メッキ層の材質は、公知の導電性金属が特に制限されずに用いられるが、一般には、上記導電性を有する硬化体を与える硬化性導電物質の材質として使用される銅等の導電性金属と同じ材質を選択するのが好ましい。また、メッキ層の厚みは、特に制限はされないが、通常５０μｍ以下の厚みで、好ましくは５μｍ～３５μｍ程度で行うのがよい。

【００１９】前記のエッチングレジストはドライフィルム、レジストインク等が特に制限無く使用され、パターンのファイン度によって適宜選択して使用すればよい。また、エッチングレジストパターンはエッチング法によってポジパターン或いはネガパターンを適宜採用すればよい。例えば、テンティング法に代表されるエッチング法ではポジパターンを、半田剥離法、ＳＥＳ法に代表されるエッチング法ではネガパターンを採用すればよい。

【００２０】本発明の多層回路基板の第１の配線パターン上には、絶縁層が形成される。上記の絶縁層は、後記する第２の配線パターンと電気的に接続される前記した第１の配線パターンの所定の部分を除いて形成される。絶縁層より露出する部分の大きさは、第１の配線パターンと第２の配線パターン及びスルーホールとの電気的接続がとれる程度でよく、具体的に例示すると、相当径が５０μｍ以上好ましくは１００μｍ以上露出すればよい。また露出する部分の形状は特に限定されず、円形、長方形、正方形等配線パターンの設計に適した形状を適宜採用すればよい。

【００２１】また、絶縁層の形成方法は、特に限定されず、公知の方法が制限無く採用される。一般にはドライフィルム、液状レジスト、ドライフィルム・液状レジスト併用等の種々の形態の硬化性絶縁樹脂を使用した方法が採用される。上記の方法で、特にドライフィルムを用いると、絶縁樹脂層の厚み精度もよく、表・裏面同時に形成できるため、より効率的に絶縁層を形成することができる。また、該絶縁層のイメージング方法としては、印刷法、写真法等をファイン度によって適宜採用すればよい。

【００２２】また、上記絶縁層上には、第２の配線パターンが形成される。かかる第２の配線パターンと第１の配線パターンとの導通は、絶縁層より露出する第１の配線パターンの所定の部分において行える。また、表側の第２の配線パターンと裏側の第１の配線パターン及び第２の配線パターンとの導通は、スルーホール上の絶縁層より露出した部分を介して行えばよく、従来のように、該スルーホールを避けて近傍に接続用のビアホールを設ける必要がなく、第２の配線パターンの配線密度を高くすることが可能となった。

【００２３】上記の第２の配線パターンとしては、信号線、電源線、グラウンド線、電磁波シールド層等のパターンに特に制限されずに用いられる。絶縁層上への配線パターンの形成法は、特に制限されないが、銅ペースト、銀ペースト等に代表される硬化性導電物質を用いて、印刷法等により形成する方法、無電解メッキ、電気メッキ等で、絶縁層を含む全ての基板上にメッキ層を形成し、該メッキ層をエッチングしてパターンを形成する方法等が一般的である。

【００２４】また、本発明の多層回路基板は前記第２の配線パターン上に同様にして、更に、絶縁層及び配線パターンを順次積層することも可能である。

【００２５】また、本発明においては、得られた多層回路基板を、プリプレグを介して積層し、更に高多層化することも可能である。

【００２６】

【発明の効果】本発明の多層回路基板の製造方法によれば、絶縁基板に形成されたスルーホール部分を含む導電層が平滑に、研削されているので、該導電層上に第１の配線パターンを形成し、更に該配線パターンの上に、絶縁層及び第２の配線パターンの形成を確実に且つ精度よく行い、信頼性の高い積層回路基板を得ることができると共に、第２の配線パターンとスルーホールとの接続を該スルーホール上で直接行うことができるため、高い配線密度で多層配線基板が得られるという特徴を有する。

【００２７】

【実施例】以下、本発明を具体的に説明するために実施例を示すが、本発明はこれらの実施例に限定されるものではない。

【００２８】実施例１

図１に示す工程に従って回路基板の製造を実施した。即ち、（ａ）両面に導電層１を有する絶縁基板２として、厚さ１．６ｍｍのガラスエポキシ銅張り積層板を使用して、（ｂ）直径０．４ｍｍφの貫通孔３をドリル加工により設けた。（ｃ）該貫通孔及び基板全面に、無電解鍍金を行った後、電気鍍金を施し、厚さ２５μｍの銅鍍金層４を形成した。（ｄ）鍍金層を形成した貫通孔に、硬化性絶縁樹脂５として、市販の熱硬化性ソルダーレジストをスクリーン印刷法にて充填、硬化した。（ｅ）該硬化性絶縁樹脂を含む導電層表面を３２０番及び６００番のバフを順次使用して、研磨整面した。（ｆ）次に、該無電解鍍金及び電気鍍金を施して、厚さ１５μの鍍金層４を形成した。（ｇ）上記鍍金層表面に、エッチングレジストインクを用いて、エッチングレジスト層を形成し、塩化第２鉄エッチング溶液でエッチングを行い、エッチングレジスト層を剥離して、第１の配線パターン６を形成した。（ｈ）該第１の配線パターン上に、絶縁層７として、感光性絶縁レジストを塗布し、露光、現像して絶縁層を形成した。次に、（ｉ）基板表面に無電解メ

ッキ、電気メッキを施し、厚み１０μｍのメッキ層を形成した。次いで、上記（ｇ）の工程に準じて第２の配線パターン８を形成した。

【００２９】得られた多層回路基板の表裏に位置し、且つ共通するスルーホールに接続する第２の配線パターン間について、ＪＩＳ，Ｃ－５０１２のホットオイル試験（２０℃×２０秒←→２６０℃５秒のサイクル）を実施した。サイクル数５００回においてでも、上記の多層回路基板の表裏に位置する第２の配線パターン間の導通は取られており、抵抗の上昇はみられなかった。

【図面の簡単な説明】

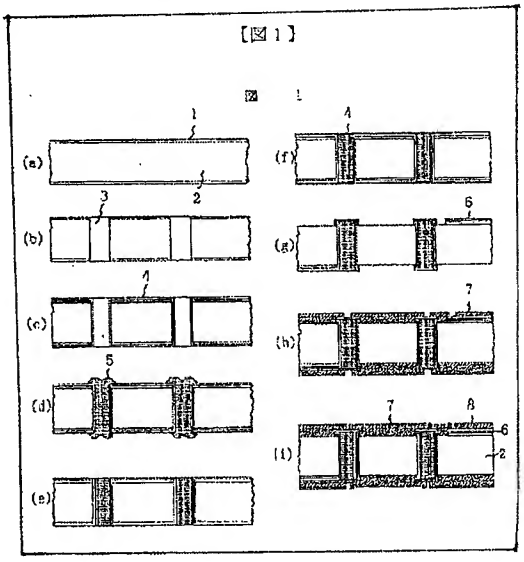
【図１】　図１は、本発明の方法の代表的な態様を示す工程図である。

【図２】　図２は、従来技術によって得られる多層回路基板の断面図である。

【符号の説明】

1　導電層
2　絶縁基板
3　貫通孔
4　鍍金層
5　硬化性絶縁樹脂
6　第１の配線パターン
7　絶縁層
8　第２の配線パターン

【図１】



【図２】